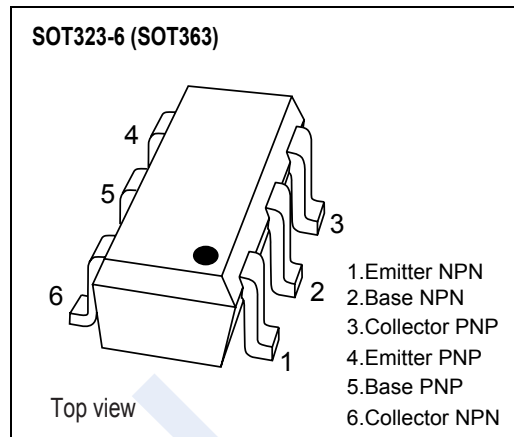
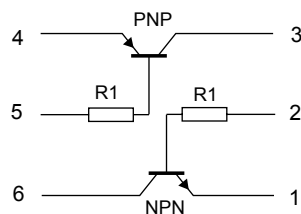


NPN/PNP Resistor-Equipped Transistors

PUMD6

■ Features

- Built-in bias resistors
- Simplified circuit design
- Reduction of component count
- Reduced pick and place costs.

■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Collector - Base Voltage	V_{CBO}	50	V
Collector - Emitter Voltage	V_{CEO}	50	
Emitter - Base Voltage	V_{EBO}	5	
Output current (DC)	I_o	100	mA
Peak Collector Current	I_{CM}	100	
Collector Power Dissipation (Note.1) Per device (Note.1)	P_C	200	mW
		300	
Thermal Resistance From (Note.1) Junction To Ambient Per device (Note.1)	$R_{th(j-a)}$	625	K/W
		416	
Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to 150	

Note.1: Transistor mounted on an FR4 printed-circuit board, single-sided copper, standard footprint.

NPN/PNP Resistor-Equipped Transistors

PUMD6

■ Electrical Characteristics Ta = 25°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Collector- base breakdown voltage	V _{CBO}	I _C = 100 μA, I _E = 0	50			V
Collector- emitter breakdown voltage	V _{CEO}	I _C = 1 mA, I _B = 0	50			
Emitter - base breakdown voltage	V _{EBO}	I _E = 100 μA, I _C = 0	5			
Collector-base cut-off current	I _{CBO}	V _{CB} = 50 V, I _E = 0			100	nA
Collector- emitter cut-off current	I _{CEO}	V _{CE} = 30 V, I _B = 0			1	uA
		V _{CE} = 30 V, I _B = 0, T _j =150°C			50	
Emitter cut-off current	I _{EBO}	V _{EB} = 5V, I _C =0			100	nA
Collector-emitter saturation voltage	V _{CE(sat)}	I _C =5 mA, I _B =0.25mA			100	mV
DC current gain	h _{FE}	V _{CE} = 5V, I _C = 1mA	200			
Input Resistor	R1		3.3	4.7	6.1	KΩ
Collector output capacitance	C _{ob}	V _{CB} = 10V, I _E = I _e =0, f=1MHz			2.5	pF
					3	

■ Marking

Marking	D*6
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NPN/PNP Resistor-Equipped Transistors

PUMD6

■ Typical Application

Plastic surface-mounted package; 6 leads

