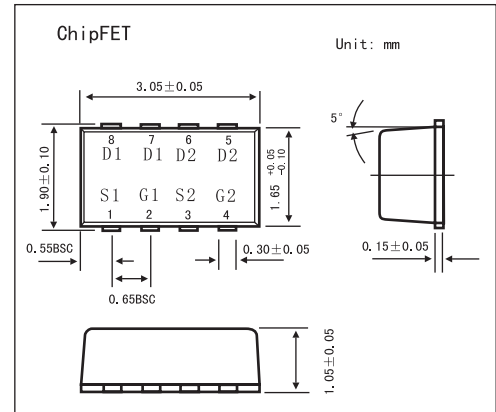
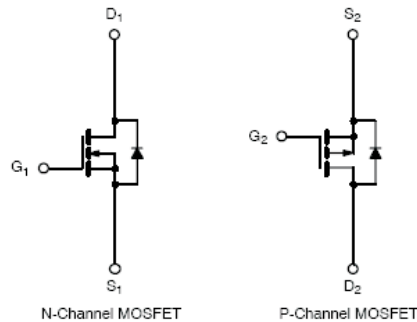


## Complementary 20-V (D-S) MOSFET

## KI5515DC

## ■ Features

- TrenchFET Power MOSFETS
- Ultra Low  $r_{DS(on)}$  and Excellent Power Handling In Compact Footprint

■ Absolute Maximum Ratings  $T_A = 25^\circ\text{C}$ 

Parameter	Symbol	N-Channel		P-Channel		Unit
		5 secs	Steady State	5 secs	Steady State	
Drain-Source Voltage	$V_{DS}$	20		-20		V
Gate-Source Voltage	$V_{GS}$	$\pm 8$				V
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ )* $T_A = 25^\circ\text{C}$	$I_D$	5.9	4.4	-4.1	-3	A
		$T_A = 85^\circ\text{C}$	4.2	3.1	-2.9	-2.2
Pulsed Drain Current	$I_{DM}$	20		-15		A
Continuous Source Current (Diode Conduction)*	$I_S$	1.8	0.9	-1.8	-0.9	A
Maximum Power Dissipation* $T_A = 25^\circ\text{C}$	$P_D$	2.1	1.1	2.1	1.1	W
		$T_A = 85^\circ\text{C}$	1.1	0.6	1.1	0.6
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150				$^\circ\text{C}$

\*Surface Mounted on 1" X 1" FR4 Board.

## ■ Thermal Resistance Ratings

Parameter	Symbol	Typ	Max	Unit	
Maximum Junction-to-Ambient*	$R_{thJA}$	$t \leq 5 \text{ sec}$	50	60	$^\circ\text{C/W}$
		Steady State	90	110	
Maximum Junction-to-Case (Drain)	$R_{thJF}$	30	40		

\*Surface Mounted on 1" X 1" FR4 Board.

## KI5515DC

■ Electrical Characteristics T<sub>J</sub> = 25°C

Parameter	Symbol	Testconditions	Min	Typ	Max	Unit
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	N-Ch	0.4	1.0	V
		V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	P-Ch	-0.4	-1.0	
Gate Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±8 V	N-Ch		±100	nA
		V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±8V	P-Ch		±100	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0 V	N-Ch		1	μA
		V <sub>DS</sub> = -20V, V <sub>GS</sub> = 0 V	P-Ch		-1	
		V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 85°C	N-Ch		5	μA
		V <sub>DS</sub> = -20V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 85°C	P-Ch		-5	
On State Drain Currenta	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 4.5 V	N-Ch	20		A
		V <sub>DS</sub> ≤ -5 V, V <sub>GS</sub> = -4.5 V	P-Ch	-15		
Drain Source On State Resistance*	r <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 4.4A	N-Ch	0.032	0.040	Ω
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -3.0A	P-Ch	0.069	0.086	
		V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 4.1A	N-Ch	0.036	0.045	
		V <sub>GS</sub> = -2.5 V, I <sub>D</sub> = -2.5A	P-Ch	0.097	0.121	
		V <sub>GS</sub> = 1.8 V, I <sub>D</sub> = 1.9A	N-Ch	0.042	0.052	
		V <sub>GS</sub> = -1.8 V, I <sub>D</sub> = -0.6A	P-Ch	0.137	0.171	
Forward Transconductance*	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 4.4A	N-Ch	22		S
		V <sub>DS</sub> = -10 V, I <sub>D</sub> = -3A	P-Ch	8		
Diode Forward Voltage*	V <sub>SD</sub>	I <sub>S</sub> = 0.9A, V <sub>GS</sub> = 0 V	N-Ch	0.8	1.2	V
		I <sub>S</sub> = -0.9A, V <sub>GS</sub> = 0 V	P-Ch	-0.8	-1.2	
Total Gate Charge	Q <sub>g</sub>	N-Channel V <sub>DS</sub> = 10V, V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 4.4A	N-Ch	5	7.5	nC
Gate Source Charge	Q <sub>gs</sub>	P-Channel	N-Ch	0.85		
Gate Drain Charge	Q <sub>gd</sub>		V <sub>DS</sub> = -10 V, V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -3A	P-Ch	0.91	
		N-Ch		1		
Turn On Time	t <sub>d(on)</sub>	N Channel V <sub>DD</sub> = 10 V, R <sub>L</sub> = 10 Ω	N-Ch	20	30	ns
Rise Time	t <sub>r</sub>	I <sub>D</sub> = 1A, V <sub>GEN</sub> = 4.5V, R <sub>g</sub> = 6 Ω	P-Ch	18	30	
			N-Ch	36	55	
Turn Off Delay Time	t <sub>d(off)</sub>	P-Channel V <sub>DD</sub> = -10 V, R <sub>L</sub> = 10 Ω	N-Ch	30	45	
			P-Ch	42	65	
Fall Time	t <sub>f</sub>	I <sub>D</sub> = -1 A, V <sub>GEN</sub> = -4.5 V, R <sub>g</sub> = 6 Ω	N-Ch	12	20	
			P-Ch	26	40	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 0.9 A, di/dt = 100 A/μs	N-Ch	45	90	
		I <sub>F</sub> = -0.9 A, di/dt = 100 A/μs	P-Ch	30	60	

\* Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.