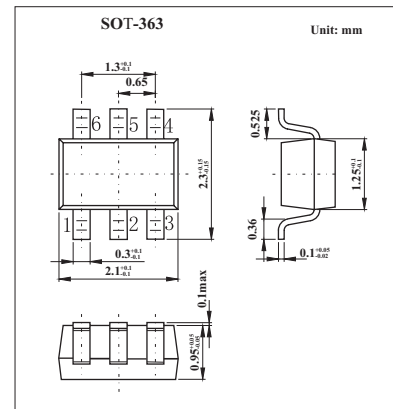
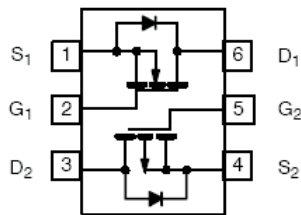


Complementary 20-V (D-S) Low-Threshold MOSFET

KI1501DL

■ PIN Configuration

■ Absolute Maximum Ratings $T_A = 25^\circ\text{C}$

Parameter	Symbol	N-Channel	P-Channel	Unit	
Drain-Source Voltage	V_{DS}	20	-20	V	
Gate-Source Voltage	V_{GS}	± 8	± 8	V	
Continuous Drain Current ($T_J = 150^\circ\text{C}$)* $T_A = 25^\circ\text{C}$	I_D	250	-180	mA	
		$T_A = 70^\circ\text{C}$	200	-140	mA
Pulsed Drain Current	I_{DM}	500	-500	mA	
Maximum Power Dissipation*	P_D	$T_A = 25^\circ\text{C}$		0.2	W
		$T_A = 70^\circ\text{C}$		0.13	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$	
Maximum Junction-to-Ambient*	R_{thJA}	625		$^\circ\text{C/W}$	

*Surface Mounted on FR4 Board, $t \leq 10$ sec.

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■ Electrical Characteristics $T_J = 25^\circ\text{C}$

Parameter	Symbol	Testconditions	Min	Typ	Max	Unit	
Drain Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 10\ \mu\text{A}$	N-Ch	20	24		V
		$V_{GS} = 0\text{ V}, I_D = -10\ \mu\text{A}$	P-Ch	-20	-24		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 50\ \mu\text{A}$	N-Ch	0.4	0.9	1.5	
		$V_{DS} = V_{GS}, I_D = -50\ \mu\text{A}$	P-Ch	-0.4	-0.9	-1.5	
Gate Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$	N-Ch		± 2	± 100	nA
			P-Ch		± 2	± 100	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$	N-Ch		0.001	100	nA
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$	P-Ch		-0.001	-100	
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55^\circ\text{C}$	N-Ch			1	μA
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55^\circ\text{C}$	P-Ch			-1	
On State Drain Currenta	$I_{D(on)}$	$V_{DS} \geq 2.5\text{ V}, V_{GS} = 5.0\text{ V}$	N-Ch	120			mA
		$V_{DS} \leq -2.5\text{ V}, V_{GS} = -5.0\text{ V}$	P-Ch	-120			
		$V_{DS} \geq 4.5\text{ V}, V_{GS} = 8.0\text{ V}$	N-Ch	400			
		$V_{DS} \leq -4.5\text{ V}, V_{GS} = -8.0\text{ V}$	P-Ch	-400			
Drain Source On State Resistance*1	$r_{DS(on)}$	$V_{GS} = 2.5\text{ V}, I_D = 150\text{ mA}$	N-Ch		1.6	2.5	Ω
		$V_{GS} = -2.5\text{ V}, I_D = -75\text{ mA}$	P-Ch		4	5	
		$V_{GS} = 4.5\text{ V}, I_D = 250\text{ mA}$	N-Ch		1.2	2.0	
		$V_{GS} = -4.5\text{ V}, I_D = -180\text{ mA}$	P-Ch		2.6	3.8	
Forward Transconductance*1	g_{fs}	$V_{DS} = 2.5\text{ V}, I_D = 50\text{ mA}$	N-Ch		150		mS
		$V_{DS} = -2.5\text{ V}, I_D = -50\text{ mA}$	P-Ch		200		
Diode Forward Voltage*1	V_{SD}	$I_S = 50\text{ mA}, V_{GS} = 0\text{ V}$	N-Ch		0.7	1.2	V
		$I_S = -50\text{ mA}, V_{GS} = 0\text{ V}$	P-Ch		-0.7	-1.2	
Total Gate Charge	Q_g	N-Channel $V_{DS} = 5\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 100\text{ mA}$	N-Ch		300	450	pC
Gate Source Charge	Q_{gs}	P-Channel $V_{DS} = -5\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -\text{mA} *2$	N-Ch		25		
			P-Ch		25		
Gate Drain Charge	Q_{gd}		N-Ch		100		
			P-Ch		100		
Input Capacitance	C_{iss}	N-Channel $V_{DS} = 5\text{ V}, V_{GS} = 0\text{ V}$	N-Ch		15		pF
			P-Ch		15		
Output Capacitance	C_{oss}	P-Channel $V_{DS} = -5\text{ V}, V_{GS} = 0\text{ V} *2$	N-Ch		11		
			P-Ch		11		
Reverse Transfer Capacitance	C_{rss}		N-Ch		5		
			P-Ch		5		
Turn On Time	$t_{d(on)}$	N Channel $V_{DD} = 3\text{ V}, R_L = 100\ \Omega$	N-Ch		7	12	ns
Rise Time	t_r	$I_D = 0.25\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 10\ \Omega$	N-Ch		25	35	
			P-Ch		25	35	
Turn Off Delay Time	$t_{d(off)}$	P-Channel $V_{DD} = -3\text{ V}, R_L = 100\ \Omega$	N-Ch		19	30	
			P-Ch		19	30	
Fall Time	t_f	$I_D = -0.25\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 10\ \Omega$	N-Ch		9	15	
			P-Ch		9	15	

*1 Guaranteed by design, not subject to production testing.

*2 Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.