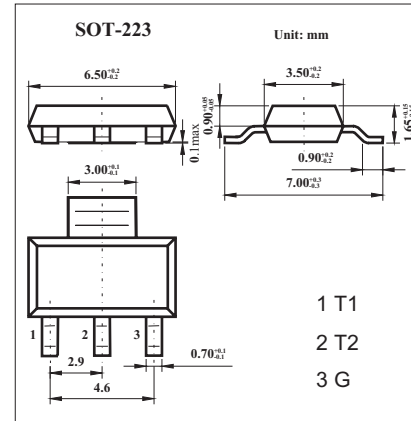
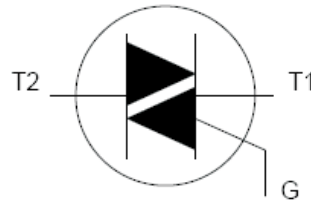


## Triacs

### BT134W Series

#### ■ Features

- Repetitive peak off-state voltages : $V_{DRM}=500V\sim 800V$
- RMS on-state current : $I_{T(RMS)}=1A$
- Non-repetitive peak on-state current : $I_{TSM}=10A$



#### ■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	Testconditions	BT134W-500	BT134W-600	BT134W-800	Unit
Repetitive peak off-state voltages	$V_{DRM}$		500	600	800	V
RMS on-state current	$I_{T(RMS)}$	full sine wave; $T_{mb} \leq 108^\circ\text{C}$	1			A
Non-repetitive peak on-state current	$I_{TSM}$	full sine wave; $T_j = 25^\circ\text{C}$ prior to surge				A
		$t = 20\text{ ms}$ $t = 16.7\text{ ms}$	10 11			A
$I^2t$ for fusing	$I^2t$	$t = 10\text{ ms}$	0.5			$\text{A}^2\text{S}$
Repetitive rate of rise of on-state current after triggering	$di_T/dt$	$I_{TM} = 1.5\text{ A}$ ; $I_G = 0.2\text{ A}$ ; $di_G/dt = 0.2\text{ A}/\mu\text{s}$	T2+ G+	50		$\text{A}/\mu\text{s}$
			T2+ G-	50		$\text{A}/\mu\text{s}$
			T2- G-	50		$\text{A}/\mu\text{s}$
			T2- G+	10		$\text{A}/\mu\text{s}$
Peak gate current	$I_{GM}$		2			A
Peak gate voltage	$V_{GM}$		5			V
Peak gate power	$P_{GM}$		5			W
Average gate power	$P_{G(AV)}$	over any 20 ms period	0.5			W
Storage temperature	$T_{stg}$		-40 to 150			$^\circ\text{C}$
Operating junction temperature	$T_j$		125			$^\circ\text{C}$
Thermal resistance junction to solder point	$R_{th\ j-sp}$	full or half cycle	15			K/W
Thermal resistance junction to ambient	$R_{th\ j-a}$	pcb mounted; minimum footprint	156			K/W
		pcb mounted;	70			K/W

## BT134W Series

## ■ Electrical Characteristics Ta = 25°C

Parameter	Symbol	Testconditions	Min			Typ	Max			Unit
			... E	... F	... G		... E	... F	... G	
Gate trigger current	I <sub>GT</sub>	V <sub>D</sub> = 12 V; I <sub>T</sub> = 0.1 A	T2+ G+			5	35	25	50	mA
			T2+ G-			8	35	25	50	mA
			T2- G-			11	35	25	50	mA
			T2- G+			30	70	70	100	mA
Latching current	I <sub>L</sub>	V <sub>D</sub> = 12 V; I <sub>GT</sub> = 0.1 A	T2+ G+			7	20	20	30	mA
			T2+ G-			16	30	30	45	mA
			T2- G-			5	20	20	30	mA
			T2- G+			7	30	30	45	mA
Holding current	I <sub>H</sub>	V <sub>D</sub> = 12 V; I <sub>GT</sub> = 0.1 A			5	15	15	30	mA	
On-state voltage	V <sub>T</sub>	I <sub>T</sub> = 2 A			1.2	1.5			V	
Gate trigger voltage	V <sub>GT</sub>	V <sub>D</sub> = 12 V; I <sub>T</sub> = 0.1 A				0.7	1.5			V
		V <sub>D</sub> = 400 V; I <sub>T</sub> = 0.1 A	0.25			0.4				V
Off-state leakage current	I <sub>D</sub>	V <sub>D</sub> = V <sub>DRM(max)</sub> ; T <sub>j</sub> = 125°C			0.1	0.5			mA	
Critical rate of rise of off-state voltage	dV <sub>D</sub> /dt	V <sub>DM</sub> = 67% V <sub>DRM(max)</sub> ; T <sub>j</sub> = 125 °C ; exponential waveform; gate open circuit	100	50	200	250				V/μs
Critical rate of change of commutating voltage	dV <sub>com</sub> /dt	V <sub>DM</sub> = 400 V; T <sub>j</sub> = 95 °C ; I <sub>T(RMS)</sub> = 1A; dI <sub>com</sub> /dt = 1.8 A/ms; gate open circuit			10	50				V/μs
Gate controlled turn-on time	t <sub>gt</sub>	I <sub>TM</sub> = 1.5 A; V <sub>D</sub> = V <sub>DRM(max)</sub> ; I <sub>G</sub> = 0.1 A; dI <sub>G</sub> /dt = 5 A/μs;				2				μs

BT134W Series

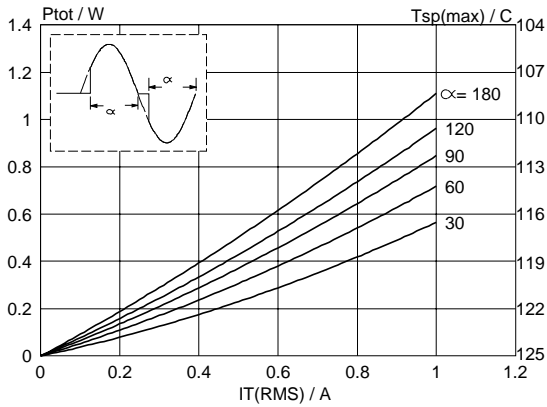


Fig.1. Maximum on-state dissipation,  $P_{tot}$ , versus rms on-state current,  $I_{T(RMS)}$ , where  $\alpha$  = conduction angle.

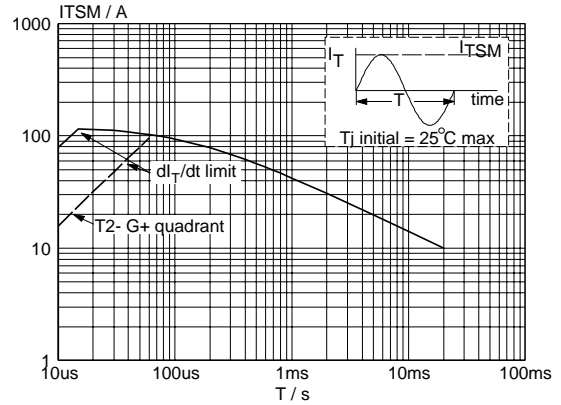


Fig.2. Maximum permissible non-repetitive peak on-state current  $I_{TSM}$ , versus pulse width  $t_p$ , for sinusoidal currents,  $t_p \leq 20ms$ .

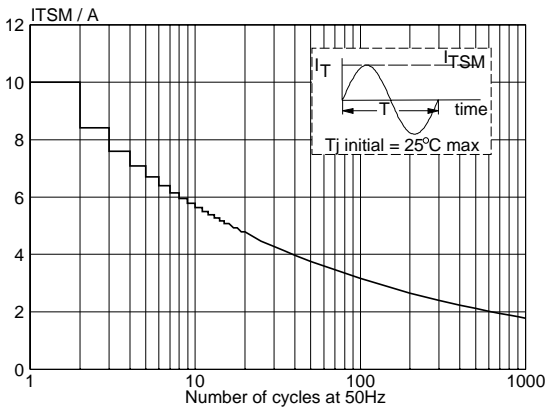


Fig.3. Maximum permissible non-repetitive peak on-state current  $I_{TSM}$ , versus number of cycles, for sinusoidal currents,  $f = 50$  Hz.

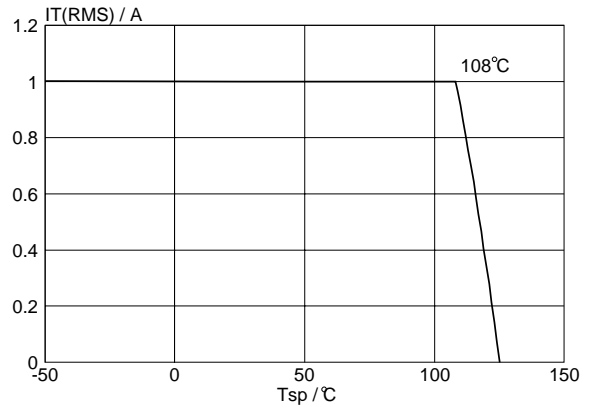


Fig.4. Maximum permissible rms current  $I_{T(RMS)}$ , versus solder point temperature  $T_{sp}$ .

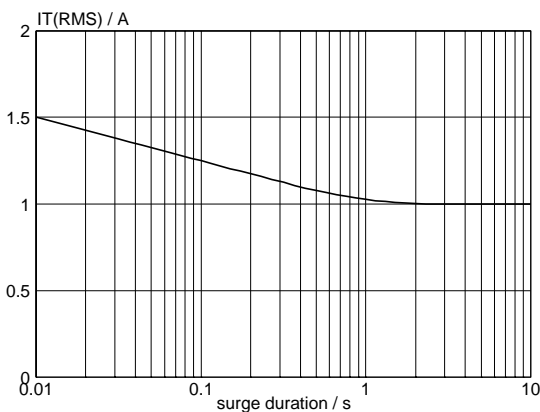


Fig.5. Maximum permissible repetitive rms on-state current  $I_{T(RMS)}$ , versus surge duration, for sinusoidal currents,  $f = 50$  Hz;  $T_{sp} \leq 108$  °C.

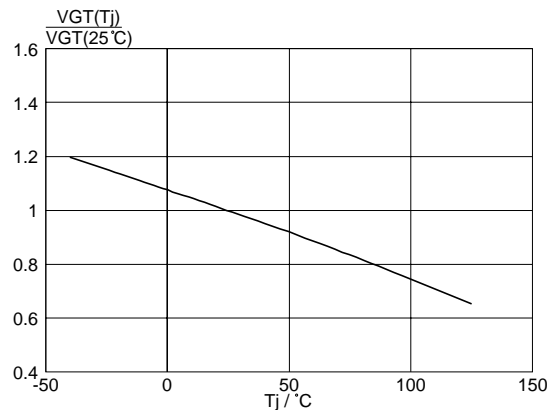


Fig.6. Normalised gate trigger voltage  $V_{GT}(T_j) / V_{GT}(25$  °C), versus junction temperature  $T_j$ .

BT134W Series

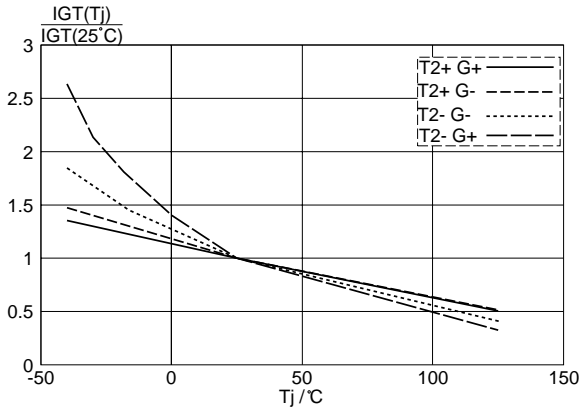


Fig. 7. Normalised gate trigger current  $I_{GT}(T_j) / I_{GT}(25^\circ\text{C})$ , versus junction temperature  $T_j$ .

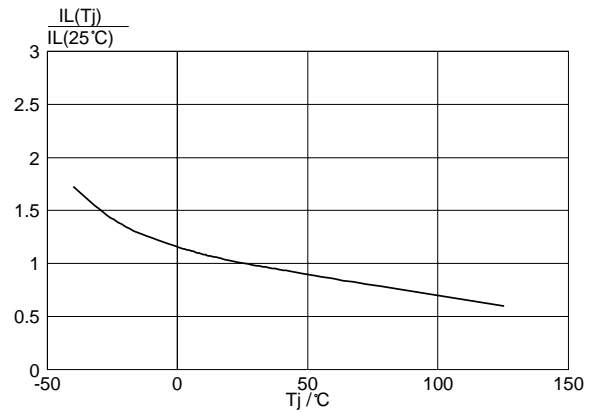


Fig. 8. Normalised latching current  $I_L(T_j) / I_L(25^\circ\text{C})$ , versus junction temperature  $T_j$ .

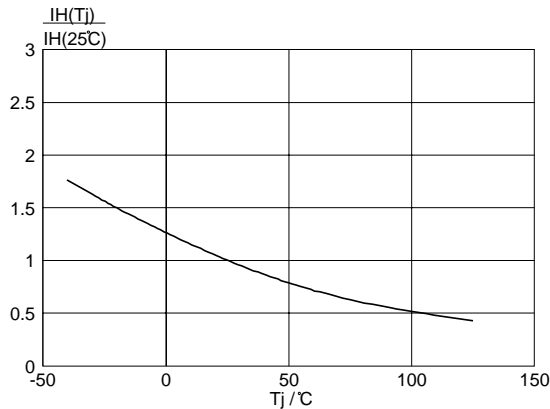


Fig. 9. Normalised holding current  $I_H(T_j) / I_H(25^\circ\text{C})$ , versus junction temperature  $T_j$ .

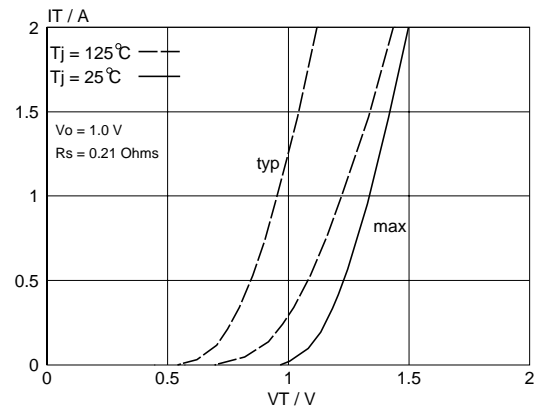


Fig. 10. Typical and maximum on-state characteristic.

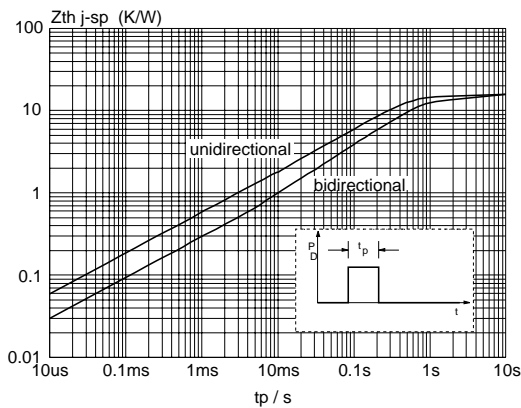


Fig. 11. Transient thermal impedance  $Z_{th\ j-sp}$ , versus pulse width  $t_p$ .

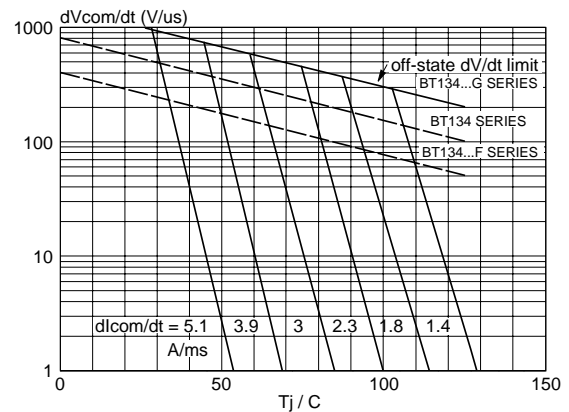


Fig. 12. Typical commutation  $dV/dt$  versus junction temperature, parameter commutation  $dl_T$  should commute when the  $dV/dt$  is below the value on the appropriate curve for pre-commutation  $dl_T/dt$ .