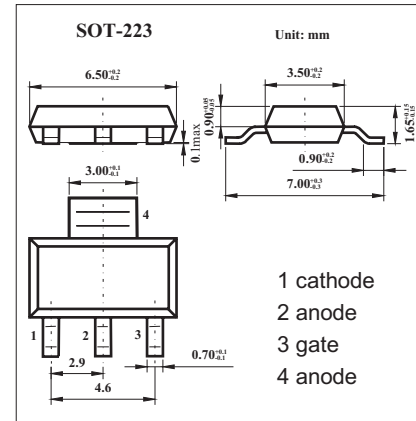
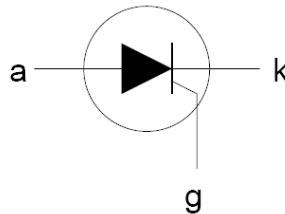


## Thyristors logic level

### BT169DW

#### ■ Features

- Designed to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits



#### ■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
repetitive peak off-state voltages	$V_{DRM}, V_{RRM}$	400	V
average on-state current half sine wave; $T_{lead} \leq 83^\circ\text{C}$	$I_{T(AV)}$	0.63	A
RMS on-state current all conduction angles	$I_{T(RMS)}$	1	A
non-repetitive peak on-state current $t = 10\text{ ms}$	$I_{TSM}$	8	A
(all conduction angles; $T_j = 25^\circ\text{C}$ ) $t = 8.3\text{ ms}$		9	A
$I^2t$ for fusing $t = 10\text{ ms}$	$I^2t$	0.32	$\text{A}^2\text{s}$
repetitive rate of rise of on-state current after triggering *	$di_T/dt$	50	$\text{A}/\mu\text{s}$
peak gate current	$I_{GM}$	1	A
peak gate voltage	$V_{GM}$	5	V
peak reverse gate voltage	$V_{RGM}$	5	V
peak gate power	$P_{GM}$	2	W
average gate power (over any 20 ms period)	$P_{G(AV)}$	0.1	W
storage temperature	$T_{stg}$	-40 to 150	$^\circ\text{C}$
junction temperature	$T_j$	125	$^\circ\text{C}$
thermal resistance from junction to ambient	$R_{th(j-a)}$	156	K/W

\*  $I_{TM} = 2\text{ A}$ ;  $I_G = 10\text{ mA}$ ;  $dI_G/dt = 100\text{ mA}/\mu\text{s}$

## BT169DW

■ Electrical Characteristics  $T_a = 25^\circ\text{C}$ 

Parameter	Symbol	Testconditions	Min	Typ	Max	Unit
gate trigger current	$I_{GT}$	$V_D = 12\text{ V}; I_T = 10\text{ mA}$		50	200	$\mu\text{ A}$
latching current	$I_L$	$V_D = 12\text{ V}; I_{GT} = 0.5\text{ mA}; R_{GK} = 1\text{ k}\Omega$		2	6	$\text{mA}$
holding current	$I_H$	$V_D = 12\text{ V}; I_{GT} = 0.5\text{ mA}; R_{GK} = 1\text{ k}\Omega$		2	5	$\text{mA}$
on-state voltage	$V_T$	$I_T = 2\text{ A}$		1.35	1.5	$\text{V}$
gate trigger voltage	$V_{GT}$	$I_T = 10\text{ mA}; V_D = 12\text{ V}$		0.5	0.8	$\text{V}$
		$I_T = 10\text{ mA}; V_D = V_{DRM(max)}; T_j = 125^\circ\text{C}$	0.2	0.3		$\text{V}$
off-state leakage current	$I_D, I_R$	$V_D = V_{DRM(max)}; V_R = V_{RRM(max)}; T_j = 125^\circ\text{C}; R_{GK} = 1\text{ k}\Omega$		0.05	0.1	$\text{mA}$
critical rate of rise of off-state voltage	$dV_D/dt$	$V_{DM} = 67\% V_{DRM(max)}; T_j = 125^\circ\text{C}; \text{exponential waveform}; R_{GK} = 1\text{ k}\Omega$	500	800		$\text{V}/\mu\text{ s}$
		$V_{DM} = 67\% V_{DRM(max)}; T_j = 125^\circ\text{C}; \text{exponential waveform}; \text{gate open circuit}$		25		$\text{V}/\mu\text{ s}$
gate controlled turn-on time	$t_{gt}$	$I_{TM} = 2\text{ A}; V_D = V_{DRM(max)}; I_G = 10\text{ mA}; di_G/dt = 0.1\text{ A}/\mu\text{ s}$		2		$\mu\text{ s}$
circuit commuted turn-off time	$t_q$	$V_D = 67\% V_{DRM(max)}; T_j = 125^\circ\text{C}; I_{TM} = 1.6\text{ A}; V_R = 35\text{ V}; di_{TM}/dt = 30\text{ A}/\mu\text{ s}; dv_D/dt = 2\text{ V}/\mu\text{ s}; R_{GK} = 1\text{ k}\Omega$		100		$\mu\text{ s}$