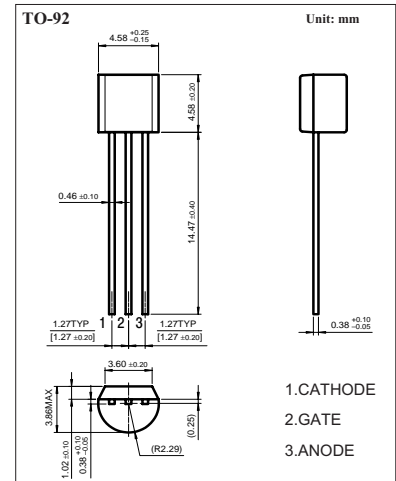
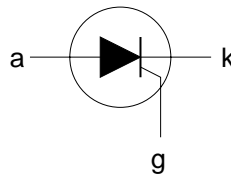


Silicon Controlled Rectifiers

BT169-600

■ Features

- Blocking voltage to 600 V
- Average on-state current to 0.5 A
- General purpose switching



■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Repetitive peak off-state voltages	V_{DRM}, V_{RRM}	600	V
Average on-state current	$I_{T(AV)}$	0.5	A
RMS on-state current	$I_{T(RMS)}$	0.8	A
Non-repetitive peak on-state current	I_{TSM}	8	A

■ Electrical Characteristics $T_a = 25^\circ\text{C}$

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Repetitive peak off-state voltages	V_{DRM}		600			V
Average on-state current	$I_{T(AV)}$	Half sine wave; $T_{lead} \leq 83^\circ\text{C}$			0.5	A
RMS on-state current	$I_{T(RMS)}$	All conduction angles			0.8	A
Non-repetitive peak on-state current	I_{TSM}	full sine wave; $T_j = 25^\circ\text{C}$ prior to surge	$t = 10\text{ ms}$		8	A
			$t = 8.3\text{ ms}$		9	A
i^2t for fusing	i^2t	$t = 10\text{ ms}$			0.32	A^2S
Repetitive rate of rise of on-state current after triggering	di_T/dt	$I_{TM} = 2\text{ A}; I_G = 10\text{ m A};$ $di_G/dt = 100\text{ m A}/\mu\text{s}$			50	$\text{A}/\mu\text{s}$
Peak gate current	I_{GM}				1	A
Peak gate voltage	V_{GM}				5	V
Peak gate power	P_{GM}				2	W
Average gate power	$P_{G(AV)}$	over any 20 ms period			0.1	W
Thermal resistance junction to ambient	$R_{\theta JA}$	PCB mounted, lead length=4mm		150		K/W
Storage temperature	T_{stg}		-40		150	$^\circ\text{C}$
Operating junction temperature	T_j				125	$^\circ\text{C}$

BT169-600

■ Electrical Characteristics $T_a = 25^\circ\text{C}$

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Gate trigger current	I_{GT}	$V_D = 12\text{ V}; I_T = 10\text{ mA}$, gate open circuit		50	200	$\mu\text{ A}$
Latching current	I_L	$V_D = 12\text{ V}; I_{GT} = 0.5\text{ mA}$ $R_{GK}=1\text{ K}\Omega$		2	6	mA
Holding current	I_H	$V_D = 12\text{ V}; I_{GT} = 0.5\text{ mA}$ $R_{GK}=1\text{ K}\Omega$		2	5	
On-state voltage	V_T	$I_T = 1\text{ A}$		1.2	1.35	V
Gate trigger voltage	V_{GT}	$V_D = 12\text{ V}; I_T = 10\text{ mA}$, gate open circuit		0.5	0.8	V
		$V_D = V_{DRM(max)}; I_T = 10\text{ mA}; T_j = 125^\circ\text{ C}$	0.2	0.3		V
Off-state leakage current	I_D, I_R	$V_D = V_{DRM(max)}; V_R = V_{RRM(max)}$ $T_j = 125^\circ\text{ C}$ $R_{GK}=1\text{ K}\Omega$		0.05	0.1	mA
Critical rate of rise of off-state voltage	dV_D/dt	$V_{DM} = 67\% V_{DRM(max)}$; $T_j = 125^\circ\text{ C}$; exponential $R_{GK}=1\text{ K}\Omega$		25		$\text{V}/\mu\text{ S}$
Gate controlled turn-on time	t_{gt}	$I_{TM}=2\text{ A}; V_D=V_{DRM(max)}$; $I_G=10\text{ mA}$ $dI_G/dt = 0.1\text{ A}/\mu\text{ s}$		2		$\mu\text{ S}$
Circuit commutated turn-off time	t_q	$I_{TM} = 1.6\text{ A}; V_D = 67\%V_{DRM(max)}$; $T_j=125^\circ\text{ C}; V_R=35\text{ V}; R_{GK}=1\text{ k}\Omega$ $dI_{TM}/dt = 30\text{ A}/\mu\text{ s}; V_D/dt = 2\text{ V}/\mu\text{ s}$		100		$\mu\text{ S}$

■ Marking

Marking	BT169-600
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BT169-600

■ Typical Characteristics

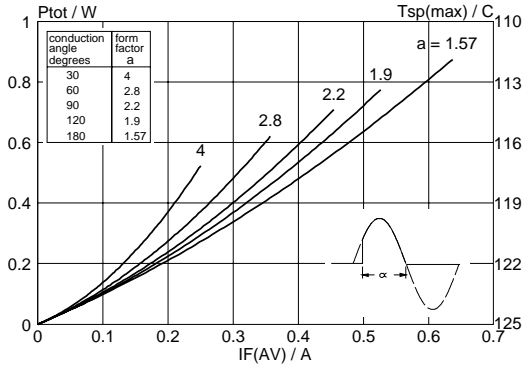


Fig.1. Maximum on-state dissipation, P_{tot} , versus average on-state current, $I_{T(AV)}$, where $a =$ form factor $= I_{T(RMS)}/I_{T(AV)}$.

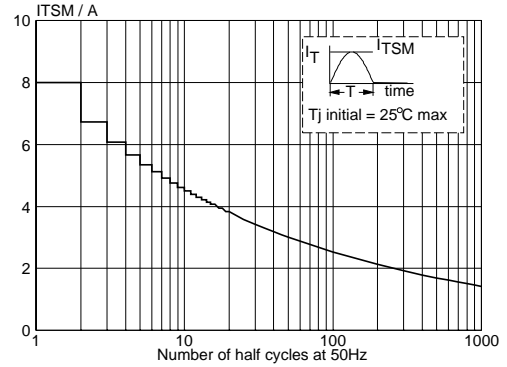


Fig.4. Maximum permissible non-repetitive peak on-state current I_{TSM} , versus number of half cycles, for sinusoidal currents, $f = 50$ Hz.

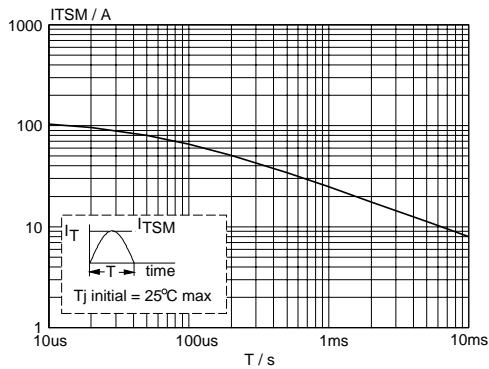


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM} , versus pulse width t_p , for sinusoidal currents, $t_p \leq 10\text{ms}$.

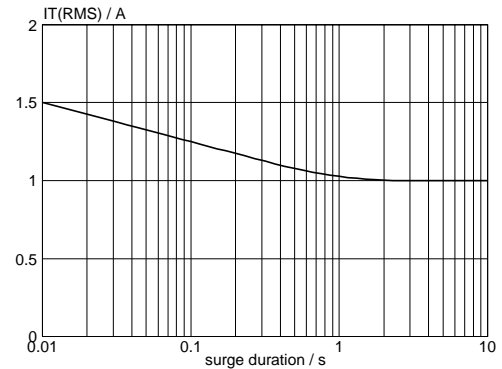


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, $f = 50$ Hz; $T_{sp} \leq 112^\circ\text{C}$.

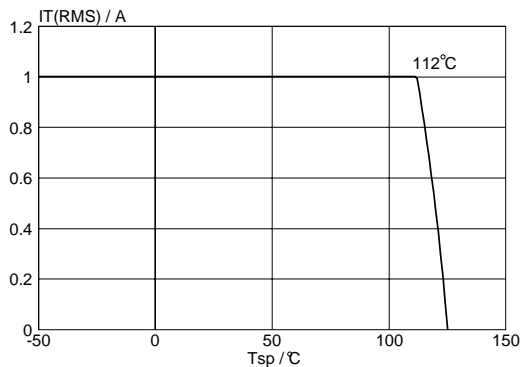


Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus solder point temperature T_{sp} .

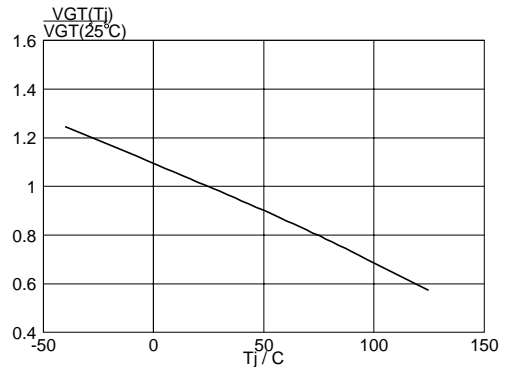


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25^\circ\text{C})$, versus junction temperature T_j .

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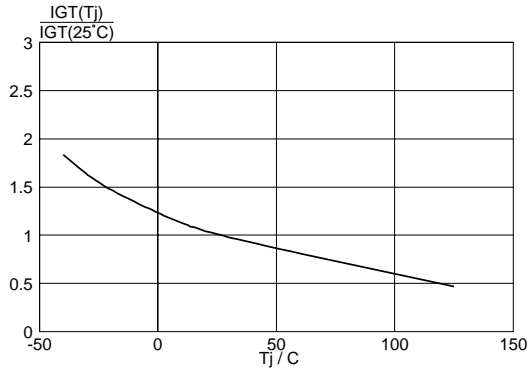


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/I_{GT}(25^\circ\text{C})$, versus junction temperature T_j .

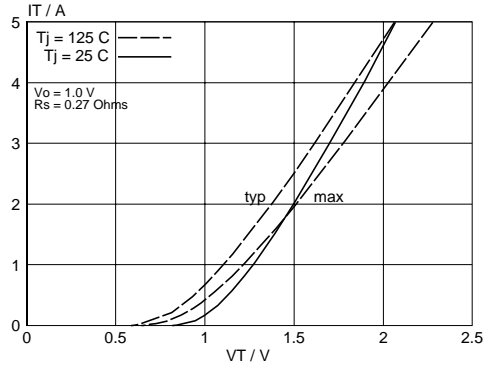


Fig.10. Typical and maximum on-state characteristic.

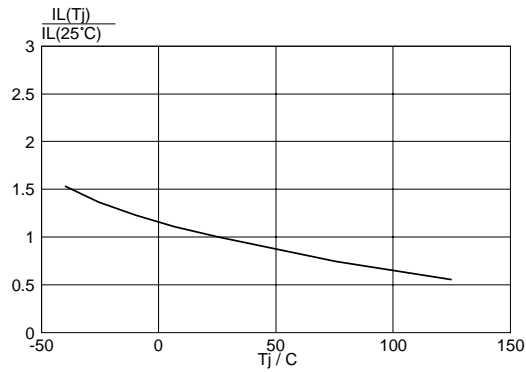


Fig.8. Normalised latching current $I_L(T_j)/I_L(25^\circ\text{C})$, versus junction temperature T_j , $R_{GK} = 1 \text{ k}\Omega$.

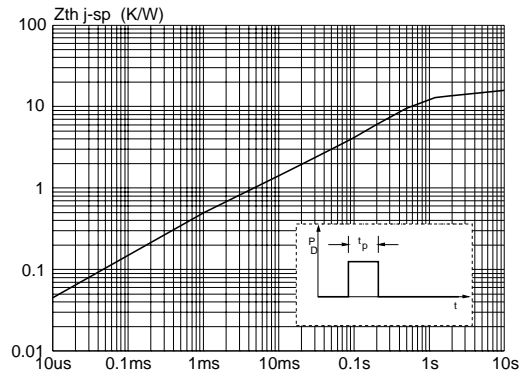


Fig.11. Transient thermal impedance $Z_{th(j-sp)}$, versus pulse width t_p .

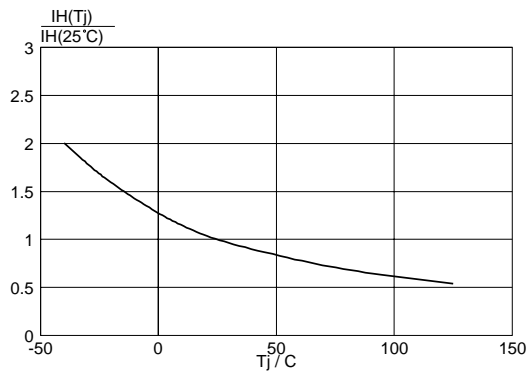


Fig.9. Normalised holding current $I_H(T_j)/I_H(25^\circ\text{C})$, versus junction temperature T_j , $R_{GK} = 1 \text{ k}\Omega$.

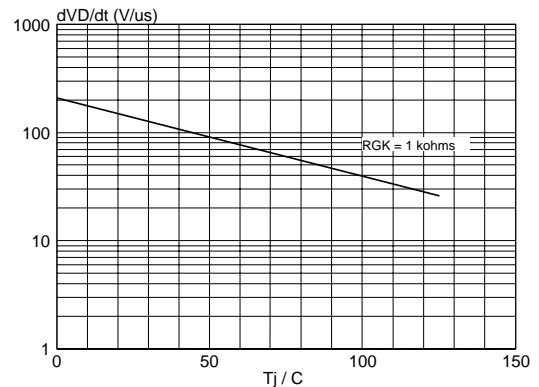


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j .